REMARKS

Claims 1-37 were previously pending in this patent application. Claims 1-37 stand rejected. Herein, no claim has been amended. Accordingly, after this Amendment and Response, Claims 1-37 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

Premature Final Rejection

It is respectfully submitted that the final rejection of Claims 1-37 made in the Office Action (mailed 11/2/2004) is premature. At page 2 of the Office Action, it is stated, "a new ground(s) of rejection is made in view of 'Low-Power Video Encoder/Decoder Chip Set for Digital VCR's' by Hasegawa et al." However, under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by Applicants' amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). See MPEP 706.07(a). Here, the new ground of rejection was neither necessitated by Applicants' amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). Thus, the final rejection of

Claims 1-37 made in the Office Action (mailed 11/2/2004) is premature. Withdrawal of the premature final rejection is respectfully requested.

Furthermore, a second or any subsequent action on the merits in any application will not be made final if it includes a rejection, on newly cited art, other than information submitted in an information disclosure statement, of any claim not amended by applicant. See MPEP 706.07(a). "Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. is newly cited art used to reject claims not amended by Applicants. Hence, the final rejection of Claims 1-37 made in the Office Action (mailed 11/2/2004) is premature. Again, withdrawal of the premature final rejection is respectfully requested.

35 U.S.C. Section 103(a) Rejections

Claims 1-3, 6-8, 10-12, 15-20, 22, 28, and 29 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. (hereafter Hasegawa) in view of Hamadani et al., U.S. Patent No. 5,845,083 (hereafter Hamadani). These rejections are respectfully traversed.

Independent Claim 1 recites:

> A method of processing digital video data for displaying, said method comprising the steps of:

a) preparsing said digital video data to recover a decoding order of said digital video data;

b) ***while preparsing said digital video data, decoding*** a variable length coding format of said preparsed digital video data; and

c) ***while decoding said variable length coding format of said preparsed digital video data, decompressing*** said decoded digital video data to facilitate displaying said digital video data on an electronic display device, wherein said ***steps a) and c) are performed according to time sharing criteria***. (emphasis added)

It is respectfully asserted that the combination of Hasegawa and Hamadani does not disclose the present invention as recited in Independent Claim 1. The Office Action cites several portions of Hasegawa and Hamadani to support the rejections under 35 U.S.C. 103(a). To the contrary, the combination of Hasegawa and Hamadani is directed to a method unlike the method recited in Independent Claim 1.

In particular, Hasegawa discloses a DV encoder algorithm and a DV decoder algorithm. Further, Figure 1 of Hasegawa shows that the shuffling, DCT compression, quantization, VL coding, and packing stages of the DV encoder algorithm are performed in a serial manner. Similarly, Figure 1 of Hasegawa shows that the unpacking, VL decoding, dequantization, IDCT decompression, and deshuffling stages of the DV decoder algorithm are performed in a serial manner. Although the Office Action states at page 2 that Hasegawa teaches the unpacking process is performed while the VL decoding is being performed, the citation (page 1784 section D, Fig. 9) used to support this assertion focuses on

the DV encoder algorithm instead of the DV decoder algorithm. The VL coding process and the packing process are described, but no discussion is made of the VL decoding and unpacking processes. Moreover, this citation simply states, "In the decoding mode, packed data flows in the opposite direction and is unpacked through formatting memory." Thus, Hasegawa fails to disclose that the unpacking (or preparsing) process is performed while the VL decoding is being performed. Further, the Office Action at page 3 acknowledges that Hasegawa does not teach performing the processes of VL decoding and decompression at the same time.

Although the Office Action states at page 3 that Hamadani teaches a MPEG compliant decoder (Figure 5) containing a control (158) for allowing the VL decoding (148) and decompression (152 and 154) to operate simultaneously, the citation (Co. 7 lines 13-31) used to support this assertion simply states, "a control finite state machine (FSM) (158) controls the decoding pipeline to enable various decoding units to operate simultaneously." The decoding units include VL decoding (148), a zigzag decoder (150), decompression (152 and 154), and a reconstruction circuit (156). The statement "to enable various decoding units to operate simultaneously" is clearly ambiguous. There is no clear teaching that the VL decoding (148) and decompression (152 and 154) are various of the decoding units that operate simultaneously. Thus, Hamadani fails to disclose that VL decoding (148) and decompression (152 and 154) operate simultaneously.

Further, the combination of Hasegawa and Hamadani does not disclose that preparsing and decompressing are performed according to time sharing criteria, as recited in Independent Claim 1.

Unlike the combination of Hasegawa and Hamadani, Independent Claim 1 is directed to a method of processing digital video data for displaying. The method includes the step of preparsing the digital video data. Additionally, the method includes the step of while preparsing the digital video data, decoding a variable length coding format of the preparsed digital video data. Furthermore, the method includes the step of while decoding the variable length coding format of the preparsed digital video data, decompressing the decoded digital video data to facilitate displaying the digital video data on an electronic display device, wherein preparsing and decompressing are performed according to time sharing criteria. As described above, the combination of Hasegawa and Hamadani fails to disclose the noted claim limitations of Independent Claim 1. Therefore, it is respectfully submitted that Independent Claim 1 is patentable over the combination of Hasegawa and Hamadani and is in condition for allowance.

Dependent Claims 2, 3, and 6-8 are dependent on allowable Independent Claim 1, which is allowable over the combination of Hasegawa and Hamadani. Hence, it is respectfully submitted that Dependent Claims 2, 3, and 6-8 are

patentable over the combination of Hasegawa and Hamadani for the reasons discussed above.

With respect to Independent Claim 10, it is respectfully submitted that Independent Claim 10 recites similar limitations as in Independent Claim 1. In particular, the computer-readable medium of Independent Claim 10 includes computer-executable instructions for performing a method of processing digital video data for displaying. The method includes the step of preparsing the digital video data. Additionally, the method includes the step of while preparsing the digital video data, decoding a variable length coding format of the preparsed digital video data. Furthermore, the method includes the step of while decoding the variable length coding format of the preparsed digital video data, decompressing the decoded digital video data to facilitate displaying the digital video data on an electronic display device, wherein preparsing and decompressing are performed according to time sharing criteria. Therefore, Independent Claim 10 is patentable over the combination of Hasegawa and Hamadani for reasons discussed in connection with Independent Claim 1.

Dependent Claims 11, 12, and 15-17 are dependent on allowable Independent Claim 10, which is allowable over the combination of Hasegawa and Hamadani. Hence, it is respectfully submitted that Dependent Claims 11, 12, and

15-17 are patentable over the combination of Hasegawa and Hamadani for the reasons discussed above.

With respect to Independent Claim 18, it is respectfully submitted that Independent Claim 18 recites similar limitations as in Independent Claim 1. In particular, the apparatus of Independent Claim 18 includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data. In particular, the variable length decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Further, the combination of Hasegawa and Hamadani discloses a formatting memory and formatting unit for preparsing (or unpacking) the digital video data instead of a processor for preparsing the digital video data. Therefore, Independent Claim 18 is patentable over the combination of Hasegawa and Hamadani for reasons discussed in connection with Independent Claim 1.

Dependent Claims 19, 20, 22, 28, and 29 are dependent on allowable Independent Claim 18, which is allowable over the combination of Hasegawa and Hamadani. Hence, it is respectfully submitted that Dependent Claims 19, 20, 22, 28 and 29 are patentable over the combination of Hasegawa and Hamadani for the reasons discussed above.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. (hereafter Hasegawa) in view of Hamadani et al., U.S. Patent No. 5,845,083 (hereafter Hamadani), and in view of Washington, U.S. Patent No. 6,389,171 (hereafter Washington). These rejections are respectfully traversed.

Dependent Claim 9 is dependent on allowable Independent Claim 1, which is allowable over the combination of Hasegawa and Hamadani. Moreover, Washington does not disclose a method of processing digital video data for displaying, as recited in Claim 1. The method includes the step of preparsing the digital video data. Additionally, the method includes the step of while preparsing the digital video data, decoding a variable length coding format of the preparsed digital video data. Furthermore, the method includes the step of while decoding the variable length coding format of the preparsed digital video data, decompressing the decoded digital video data to facilitate displaying the digital video data on an electronic display device, wherein preparsing and decompressing are performed according to time sharing criteria. Hence, it is respectfully submitted that Dependent Claim 9 is patentable over the combination of Hasegawa, Hamadani, and Washington for the reasons discussed above.

Claims 4, 5, 13, 14, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. (hereafter Hasegawa) in view of Hamadani et al., U.S. Patent No. 5,845,083 (hereafter Hamadani), and in view of Peng et al., U.S. Patent No. 6,496,199 (hereafter Peng). These rejections are respectfully traversed.

Dependent Claims 4 and 5 are dependent on allowable Independent Claim 1, which is allowable over the combination of Hasegawa and Hamadani. Moreover, Peng does not disclose a method of processing digital video data for displaying, as recited in Claim 1. The method includes the step of preparsing the digital video data. Additionally, the method includes the step of while preparsing the digital video data, decoding a variable length coding format of the preparsed digital video data. Furthermore, the method includes the step of while decoding the variable length coding format of the preparsed digital video data, decompressing the decoded digital video data to facilitate displaying the digital video data on an electronic display device, wherein preparsing and decompressing are performed according to time sharing criteria. Hence, it is respectfully submitted that Dependent Claims 4 and 5 are patentable over the combination of Hasegawa, Hamadani, and Peng for the reasons discussed above.

Dependent Claims 13 and 14 are dependent on allowable Independent Claim 10, which is allowable over the combination of Hasegawa and Hamadani. Moreover, Peng does not disclose a computer-readable medium that includes computer-executable instructions for performing a method of processing digital video data for displaying, as recited in Claim 10. The method includes the step of preparsing the digital video data. Additionally, the method includes the step of while preparsing the digital video data, decoding a variable length coding format of the preparsed digital video data. Furthermore, the method includes the step of while decoding the variable length coding format of the preparsed digital video data, decompressing the decoded digital video data to facilitate displaying the digital video data on an electronic display device, wherein preparsing and decompressing are performed according to time sharing criteria. Hence, it is respectfully submitted that Dependent Claims 13 and 14 are patentable over the combination of Hasegawa, Hamadani, and Peng for the reasons discussed above.

Dependent Claim 27 is dependent on allowable Independent Claim 18, which is allowable over the combination of Hasegawa and Hamadani. Moreover, Peng does not disclose an apparatus that includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data, as recited in Claim 18. In particular, the variable length

decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Hence, it is respectfully submitted that Dependent Claim 27 is patentable over the combination of Hasegawa, Hamadani, and Peng for the reasons discussed above.

Claims 21, 23-26, 30-34, and 36-37 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. (hereafter Hasegawa) in view of Hamadani et al., U.S. Patent No. 5,845,083 (hereafter Hamadani), and in view of Jan, U.S. Patent No. 5,363,097 (hereafter Jan). These rejections are respectfully traversed.

Dependent Claims 21 and 23-26 are dependent on allowable Independent Claim 18, which is allowable over the combination of Hasegawa and Hamadani. Moreover, Jan does not disclose an apparatus that includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data, as recited in Claim 18. In particular, the variable length decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Hence, it is respectfully submitted that Dependent Claims 21 and 23-26 are

patentable over the combination of Hasegawa, Hamadani, and Jan for the reasons discussed above.

With respect to Independent Claim 30, it is respectfully submitted that Independent Claim 30 recites similar limitations as in Independent Claim 1. In particular, the digital video data decoder of Independent Claim 30 includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data. In particular, the variable length decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Further, the combination of Hasegawa and Hamadani discloses a formatting memory and formatting unit for preparsing (or unpacking) the digital video data instead of a processor for preparsing the digital video data. Therefore, Independent Claim 30 is patentable over the combination of Hasegawa and Hamadani for reasons discussed in connection with Independent Claim 1.

Moreover, Jan does not disclose a digital video data decoder that includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data, as recited in Independent Claim 30. In particular, the variable length decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Hence, it is respectfully submitted

that Independent Claim 30 is patentable over the combination of Hasegawa, Hamadani, and Jan for the reasons discussed above.

Dependent Claims 31-34 and 36-37 are dependent on allowable Independent Claim 30, which is allowable over the combination of Hasegawa, Hamadani, and Jan. Hence, it is respectfully submitted that Dependent Claims 31-34 and 36-37 are patentable over the combination of Hasegawa, Hamadani, and Jan for the reasons discussed above.

Claim 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Low-Power Video Encoder/Decoder Chip Set for Digital VCR's" by Hasegawa et al. (hereafter Hasegawa) in view of Hamadani et al., U.S. Patent No. 5,845,083 (hereafter Hamadani), in view of Jan, U.S. Patent No. 5,363,097 (hereafter Jan), and further in view of Peng et al., U.S. Patent No. 6,496,199 (hereafter Peng). These rejections are respectfully traversed.

Dependent Claim 35 is dependent on allowable Independent Claim 30, which is allowable over the combination of Hasegawa, Hamadani, and Jan. Moreover, Peng does not disclose a digital video data decoder that includes a processor for preparsing digital video data and a variable length decoding unit for decoding the preparsed digital video data, as recited in Independent Claim 30. In

particular, the variable length decoding unit is configured to decode the variable length coding format of the preparsed digital video data while the processor preparses the digital video data. Hence, it is respectfully submitted that dependent Claim 35 is patentable over the combination of Hasegawa, Hamadani, Jan, and Washington for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above arguments and remarks overcome all rejections. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-37) are in condition for allowance.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Dated: 2/10/2005

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